

# **SoS: A Service-Oriented Scalable Traffic Control Architecture for Future Internet**

**Speaker:** Dr. Hao Che  
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**Date:** Friday, March 2, 2007

**Time:** 10 am - 12 noon

**Venue:** WH 413 (CReWMaN Lab)

## **Abstract:**

Today's Internet only offers a single packet delivery service at global scale - Best Effort (BE) service. However, to adequately support real-time applications with stringent delay and loss constraints at global scale, it is imperative to design innovative scalable architectures that support features including Fast Failure Recovery (FFR), Quality of Service (QoS), and Traffic Engineering (TE). Despite the great effort made in the past decade, there has been no large-scale deployment of such features to date.

In this talk, we will propose a Service Oriented Scalable (SoS) traffic control architecture. SOS supports an essential set of service quality features to meet real-time application needs. The idea is to develop a set of distributed, optimization-based, QoS-aware traffic controllers in a multi-domain environment. These controllers enable integrated, QoS-aware TE and FFR through dynamic load balancing and rate adaptation of traffic aggregates at two levels, single-hop at the inter-domain level and edge-to-edge at the intra-domain level. SOS is in line with the distributed routing structure and forwarding paradigm of the Internet and hence can be integrated into the basic Internet architecture to enable those service quality features at global scale.

**Speaker Bio:**

Dr. Hao Che received his Ph.D. degree in electrical engineering from the University of Texas at Austin, in 1998. He was an Assistant Professor of Electrical Engineering at the Pennsylvania State University (1998-2000) and a System Architect with Santera Systems, Inc. (2000-2002). Since Fall 2002, Dr. Che has been an Assistant Professor of Computer Science and Engineering at the University of Texas at Arlington. His current research interests include network architecture and design, network resource management, router architecture, and network processor and coprocessor design.